- **max 10 words may be read out as a whole (i.e. 20 bytes)**
- **first 160 bits can be addressed bitwise (i.e. the whole map)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0040hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	3hex
firmware MSB	2 MSB	R	firmware version upper byte	
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable	
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – reserved **bit 3** – reserved **bit 4** - 0 **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	module address	The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (communication speed)	4 MSB	R,W EEPROM	no parity 10dec … 1200 bps 11dec … 2400 bps 12dec … 4800 bps 13dec … 9600 bps 14dec … 19200 bps 15dec … 38 400bps 16dec … 57 600bps 17dec … 115 200bps	The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
input states	5 LSB	R,RAM	readouts of the inputs	bit 0...input DI1 .. bit 7...input DI8
latched value	5 MSB	R, RAM	catched values	reset of individual bits: disable and enable the

			0 – if since latch enable the latched state has not been detected at the input **1 -** if since latch enable the latched state has been detected at the input	corresponding bits – see register **latch enable** bit 0...input DI1 .. bit 7...input DI8
latch state	6 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	bit 0...input DI1 .. bit 7...input DI8
reserved	6 MSB		not used	
reserved	7 LSB		not used	
latch enable	7 MSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after RESET the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits) bit 0...input DI1 .. bit 7...input DI8
uptime 1	8 LSB	R	time in seconds since module power-up or reset	LSB
uptime 2	8 MSB	R		
uptime 3	9 LSB	R		
uptime 4	9 MSB	R		MSB
number of EE write cycles 1	10 LSB	R	number of EEPROM writing cycles (address, baud rate, range...), just for information	counter 0...FFFE; no overflow. When FFFE is reached, the counter stops.
number of EE write cycles 2	10 MSB	R		