- **max 22 words may be read out as a whole (i.e. 44 bytes)**
- **first 256 bits can be addressed bitwise (i.e. 1LSB - 16MSB)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0062hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	01
firmware MSB	2 MSB	R	firmware version upper byte	00
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** (write offset coefficient to EEPROM) change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** (write calibration span coefficient to EEPROM) change bit 7 from 1 to 0 and set bit 6 to 1
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2 -** 1 **–** EEPROM initialised **bit 3** – 1 – calibration enabled **bit 4** - 0 **bit 5** - 1 **bit 6** - 0	

			bit 7 - 1	
address	4 LSB	R,W EEPROM	module address (0x01)	The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (communication speed)	4 MSB	R,W EEPROM	no parity 10_{dec} … 1200 bps 11_{dec} … 2400 bps 12_{dec} … 4800 bps 13_{dec} … 9600 bps 14_{dec} … 19200 bps 15_{dec} … 38 400bps 16_{dec} … 57 600bps 17_{dec} … 115 200bps	The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
output range for outputs 1, 2	5 LSB	R,W EEPROM	9 … current 4 to 20 mA	bit 0 to bit 3: output 1 bit 4 to bit 7: output 2
output range for outputs 3, 4	5 MSB	R,W EEPROM		bit 0 to bit 3: output 3 bit 4 to bit 7: output 4
reserved	6 LSB	R,W RAM		
reserved	6 MSB	R,W RAM		
output 1 value	7 LSB, 7 MSB	R,W EEPROM	0...16383 according to range (0000_{hex} - $3FFF_{hex}$)	0... 4 mA 16383...20 mA
output 2 value	8 LSB, 8 MSB	R,W EEPROM		
output 3 value	9 LSB, 9 MSB	R,W EEPROM		
output 4 value	10 LSB, 10 MSB	R,W EEPROM		
reserved	11 LSB, 11 MSB	R,W RAM		
reserved	12 LSB, 12 MSB	R,W RAM		
reserved	13 LSB, 13 MSB	R,W RAM		
reserved	14 LSB, 14 MSB	R,W RAM		
offset calibration output 1	15 LSB, 15 MSB	R,W EEPROM	0...16383 according to range (0000_{hex} - $3FFF_{hex}$)	
span calibration output 1	16 LSB, 16 MSB	R,W EEPROM		
offset calibration output 2	17 LSB, 17 MSB	R,W EEPROM		

span calibration output 2	18 LSB, 18 MSB	R,W EEPROM		
offset calibration output 3	19 LSB, 19 MSB	R,W EEPROM		
span calibration output 3	20 LSB, 20 MSB	R,W EEPROM		
offset calibration output 4	21 LSB, 21 MSB	R,W EEPROM		
span calibration output 4	22 LSB, 22 MSB	R,W EEPROM		