M710 Modbus table

4 counter inputs + RTC Release 10.2.2009 ver. 100

domat control system

- **max 22 words may be read out as a whole (i.e. 44 bytes)**
- **first 224 bits can be addressed bitwise (i.e. the whole map except for RTC and count 3 and 4)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0071hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	01
firmware MSB	2 MSB	R	firmware version upper byte	00
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init (go to factory defaults)	EEPROM init: set INIT switch to ON start module set INIT switch to OFF set bit 4 to true
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – 1 – EPROM initialised **bit 3** – not used **bit 4** - 0 **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	module address (0x01)	**!!!**The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (comm speed)	4 MSB	R,W EEPROM	no parity 10dec … 1200 bps 11dec … 2400 bps 12dec … 4800 bps 13dec … 9600 bps 14dec … 19200 bps 15dec … 38400 bps 16dec … 57600 bps 17dec … 115200 bps	**!!!**The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)

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count 1	5 LSB 5 MSB 6 LSB 6 MSB	R,W NVRAM	pulse counter at CNT1	value is backed up when power off – counting input
count 2	7 LSB 7 MSB 8 LSB 8 MSB	R,W NVRAM	pulse counter at CNT2	value is backed up when power off – counting input and sync input for 15min. load shedding
actual	9 LSB 9 MSB 10 LSB 10 MSB	R,W NVRAM	pulses counted in the current 15min period; with rising edge at CNT2 this value is copied to register **last** and the **actual** register is set to zero	value is backed up when power off, after power restore the counting continues until rising edge at CNT2
last	11 LSB 11 MSB 12 LSB 12 MSB	R,W NVRAM	pulses counted in the last 15min period	value is backed up when power off
time 1/4	13 LSB 13 MSB 14 LSB 14 MSB	R,W NVRAM	time (in secs) of current 15 min. interval	when power off, the counter is paused, and continues after power restoration
count 3	15 LSB 15 MSB 16 LSB 16 MSB	R,W NVRAM	pulse counter at CNT3	value is backed up when power off – counting input
count 4	17 LSB 17 MSB 18 LSB 18 MSB	R,W NVRAM	pulse counter at CNT4	value is backed up when power off – counting input
RTC	19 LSB 19 MSB 20 LSB 20 MSB 21 LSB 21 MSB 22 LSB 22 MSB	R,W NVRAM	real time clock	see table below; to write to these registers, Write to EEPROM must be enabled – see **status LSB**

RTC Table

Addr.	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Range
15 LSB		10xsecs			seconds				secs	00-59
15 MSB	0	10xmins			minutes				mins	00-59
16 LSB	0	24	10xhours	10xhours	hours				hours	00-23
		12	AM / PM							1-12 + AM/PM
16 MSB	0	0	0	0	0	day			day	01-07
17 LSB	0	0	10xdate		date				date	01-31
17 MSB	0	0	0	10xmonth	month				month	01-12
18 LSB	10xyear				year				year	00-99
18 MSB	0	0	0	0	0	0	0	0	not used	00