MMIO Modbus table

4 DI, 7 DO, 4 AI, 2 AO Release 23.9.2011 ver. 00400

domat control system

- **max 16 words may be read out as a whole (i.e. 32 bytes)**
- **first 256 bits can be addressed bitwise (i.e. 1 LSB – 16 MSB)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0102hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	4hex
firmware MSB	2 MSB	R	firmware version upper byte	
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** change bit 7 from 1 to 0 and set bit 6 to 1
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – 1 – EPROM initialised **bit 3** – 1 – calibration enabled **bit 4** - 0 **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	module address (0x01)	The changes will become active only after module restart (the register is

				written immediately, but the new address is effective after restart)
baud rate (comm speed)	4 MSB	R,W EEPROM	no parity 10_{dec} … 1200 bps 11_{dec} … 2400 bps 12_{dec} … 4800 bps 13_{dec} … 9600 bps 14_{dec} … 19200 bps 15_{dec} … 38400 bps 16_{dec} … 57600 bps 17_{dec} … 115200 bps	The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
input range for AI1, AI2	5 LSB	R,W EEPROM	**1 …Pt1000** (-50 to 150 °C) (0 to 20000), **divide by 100 and subtract 50** to get the correct value **2 … voltage 0V … 10 V** (0 to 9999), **divide by 1000** to get the correct value – AI1 and AI2 only! **3 … resistance 0 … 1600 ohm** (0 to 16000), **divide by 10** to get the correct value **4 … current 0 … 20 mA** (0 to 2000), **divide by 100** to get the correct value – external resistor 125 Ohm necessary **5 … resistance 0 – 5000 ohm** (0 to 50000), **divide by 10** to get the correct value.	bit 0 – bit 3… channel 1 bit 4 – bit 7… channel 2
				bit 0 – bit 3… channel 3 bit 4 – bit 7… channel 4
input range for AI3, AI4	5 MSB	R,W EEPROM		bit 0 – bit 3… channel 5 bit 4 – bit 7… channel 6
				bit 0 – bit 3… channel 7 bit 4 – bit 7… channel 8
latch state	6 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	
relay com	6 MSB	R,W EEPROM	**0** – when no communication, relays stay in last state **1** – when no communication, relays are set to **relay state** values	bit 0 is relay 1 … bit 6 is relay 7
relay state	7 LSB	R,W EEPROM	relays go on or off (according to corresponding bits) if there was no communication with module for a given time and in **relay com** the corresponding relay bit is set to 1	bit 0 is relay 1 … bit 6 is relay 7
relay time	7 MSB	R,W EEPROM	time in [s] of no communication which is considered as communication failure	if set to 0, the function is disabled

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relay start enable	8 LSB	R,W EEPROM	startup relay behaviour **0** – relays are not commanded **1** – the corresponding relay is set to its **relay start** value after module startup	bit 0 is relay 1 … bit 6 is relay 7
relay start	8 MSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 1 … bit 6 is relay 7
relay	9 LSB	R, W RAM	commands to control outputs (DO1-DO7)	bit 0 is relay 1 … bit 6 is relay 7
latch enable	9 MSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after RESET the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits)
analogue outputs AO1	10 LSB	R,W RAM	the AO values are ranged 0000hex – 0FFFhex which is (0 dec – 4095dec) 0000hex is for 0V 0FFFhex is for 10V	analogue output channels
	10 MSB	R,W RAM		
analogue outputs AO2	11 LSB	R,W RAM		
	11 MSB	R,W RAM		
inputs	12 LSB	R	readout of binary inputs (DI1-DI4)	bit 0 is input 1 … bit 3 is input 4
latched value	12 MSB	R, W RAM	catched values **0 –** if since latch enable the latched state has not been detected at the input **1 -** if since latch enable the latched state has been detected at the input	reset of individual bits: disable and enable the corresponding bits – see register **latch enable**
channel value AI1	13 LSB	R RAM	measured values at analogue inputs; scaling: see **input ranges** register (reg. 5)	readouts of analogue inputs AI1..AI4
	13 MSB	R RAM		
channel value AI2	14 LSB	R RAM		
	14 MSB	R RAM		
channel value AI3	15 LSB	R RAM		
	15 MSB	R RAM		
channel value AI4	16 LSB	R RAM		
	16 MSB	R RAM		