

## MT020 Modbus table

Release 23.9.2011 ver. 100



- max 7 words may be read out as a whole (i.e. 14 bytes)
- first 128 bits can be addressed bitwise (i.e. whole map)

Register name	Address	Type	Description	Notes
module LSB	1 LSB	R	module identification lower byte	module identification 0800 <sub>hex</sub>
module MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	1hex
firmware MSB	2 MSB	R	firmware version upper byte	
status LSB	3 LSB	R, W RAM	module status lower byte <b>bit 0</b> – enables EEPROM writing	
status MSB	3 MSB	R	module status upper byte <b>bit 0</b> - 0 normal mode - 1 init mode <b>bit 1</b> - 1 at the next EEPROM write attempt will all data be written to EEPROM - 0 at the next EEPROM write attempt received data will be written to RAM only  <b>bit 2</b> reserved <b>bit 3</b> reserved <b>bit 4</b> - 1 <b>bit 5</b> - 0 <b>bit 6</b> - 1 <b>bit 7</b> - 0	
address	4 LSB	R,W EEPROM	module address (0x01)	The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate	4 MSB	R,W EEPROM	communication, no parity 10 <sub>dec</sub> ... 1 200bps 11 <sub>dec</sub> ... 2 400bps 12 <sub>dec</sub> ... 4 800bps 13 <sub>dec</sub> ... 9 600bps 14 <sub>dec</sub> ... 19 200bps	The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
inputs settings	5 LSB, MSB	R, W EEPROM (0xFFFF)	alarm configuration 0 - on respective bits: alarm active if input on low 1- on respective bits: alarm active if input on high	bit 0 = input 1 ... bit11 = input 12 bit12 = ACK bit13 = TEST

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relay settings	6 LSB, MSB	R, W EEPROM (0xFFFF)	summary relay configuration 0 – on respective bits: input does not activate the alarm summary relay 1– on respective bits: input activates the alarm summary relay	bit 0 = input 1 ... bit11 = input 12
tests	6 LSB, MSB	R,W RAM	bit 0...bit 11:Remote activation of alarms bit 12: Alarm acknowledgment bit 13: Alarm test	bit 0 = input 1 ... bit11 = input 12 bit12 = ACK bit13 = TEST
relay	8 LSB	R RAM		bit 0 – actual state summary relay
	8 MSB		reserved	
inputs	9 LSB, MSB	R RAM	actual state all digital inputs	bit 0 = input 1 ... bit11 = input 12 bit12 = ACK bit13 = TEST
alarms	10 LSB, MSB	R RAM	Triggered alarms (active or inactive) which are still waiting to be acknowledged (button or via Modbus) After acknowledging the register is set to 0.	bit 0 = input 1 ... bit11 = input 12