MTala010 Modbus table
8 DI, 6 alarm LED,
beep, reset button

Release 10.2.2009 ver. 100

domat
control system

- **max 7 words may be read out as a whole (i.e. 14 bytes)**
- **first 112 bits can be addressed bitwise (i.e. whole map)**

Register name	Address	Type	Description	Notes
module LSB	1 LSB	R	module identification lower byte	module identification 0120hex
module MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	value 01
firmware MSB	2 MSB	R	firmware version upper byte	value 00
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – enables EEPROM writing	
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt will all data be written to EEPROM - 0 at the next EEPROM write attempt received data will be written to RAM only **bit 2** reserved **bit 3** reserved **bit 4** - 1 **bit 5** - 0 **bit 6** - 1 **bit 7** - 0	
address	4 LSB	R,W EEPROM	module address	The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate	4 MSB	R,W EEPROM	communication, no parity 10deci … 1 200bps 11deci … 2 400bps 12deci … 4 800bps 13deci … 9 600bps 14deci … 19 200bps 15deci … 38 400bps 16deci … 57 600bps 17deci … 115 200bps	The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
inputs	5 LSB	R	input readouts	bit 0 = input 1 … bit 7 = input 8

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latched values	5 MSB	R	latched values **0 –** after **latch enable** there has not been active state at the bits **1 -** after **latch enable** there has been active state at the bits	reset the bits by latch disabling and enabling - see **latch enable** bit 0 = input 1 … bit 7 = input 8
latch state	6 LSB	R,W EEPROM	state to be considered as active **0** – log. 0 will be catched **1** – log. 1 will be catched	
input as alarm	6 MSB	R,W EEPROM	enable the input as alarm (applies for DI1 to DI6) **0** – the input is not an alarm input **1** – the input is an alarm input	
alarm	7 LSB	R,W RAM	**alarm register (applies for bit 0 to bit 5 and bit 7)** **bit 0 to bit 5 – 1 alarm is active** **bit 0 to bit 5 – 0 alarm is inactive** **bit 6 – 1** disable beep when alarm active **bit 6 – 0** enable beep when alarm active	by writing **1** to a particular bit an alarm is invoked, which remains until the acknowledge button is pushed
latch enable	7 MSB	R,W RAM	enable latch for each input separately – write **1** to set the **latched value** for the corresponding bit to log. 0. The bit remains in 0 until the corresponding input is active. After reboot, the complete register is set to 0.	Reset the catched bits in the **latched value** register by disable and enable the bits in the **latch enable** register.