MXIO Modbus table

32 DI, 32 DO, 16 AI, 8 AO Release 22.5.2014 ver. 00801

domat control system

- **max 53 words may be read out as a whole (i.e. 106 bytes)**
- **first 848 bits can be addressed bitwise (i.e. 1LSB – 53MSB)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0103hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	lower byte FW version	8hex
firmware MSB	2 MSB	R	upper byte FW version	
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB)
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – 1 – EPROM initialised **bit 4** – 0 –correct on-board I2C communication between processor and peripherals - 1 –incorrect on-board I2C communication between processor and peripherals **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	Modbus module address **default address for MXIO is 1** **default address for MXPLC is 2**	**!!!** the change will be effective after restart only (however the register will be set immediately)

baud rate	4 MSB	R,W EEPROM	no parity communication 10dec … 1200bps 11dec … 2400bps 12dec … 4800bps 13dec … 9600bps 14dec … 19200bps	**!!!** the change will be effective after restart only (however the register will be set immediately)
calibration 1	5 LSB	R,W RAM	register to calibrate analogue inputs 1-8 **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** change bit 7 from 1 to 0 and set bit 6 to 1
calibration 1	5 MSB	R,W RAM	**bit 3** – 1 - calibration enable	indicates enabled calibration of analogue inputs 1-8
calibration 2	6 LSB	R,W RAM	register to calibrate analogue inputs 9-16 **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	function is same as calibration 1 LSB
calibration 2	6 MSB	R,W RAM	bit 3 – 1 - calibration enable	indicates enabled calibration of analogue inputs 9-16
input range for AI1, AI2	7 LSB	R,W EEPROM	**1 …Pt1000** (-50 to 150 °C) (-5000 to 15000), **divide by 100** to get the correct value **3 … resistance 0 … 1600 ohm** (0 to 16000), **divide by 10** to get the correct value **5 … resistance 0 – 5000 ohm** (0 to 50000), **divide by 10** to get the correct value.	bit 0 – bit 3…channel 1 … bit 4 – bit 7… channel 2
input range for AI3, AI4	7 MSB	R,W EEPROM		bit 0 – bit 3… channel 3 … bit 4 – bit 7… channel 4
input range for AI5, AI6	8 LSB	R,W EEPROM		bit 0 – bit 3… channel 5 … bit 4 – bit 7… channel 6
input range for AI7, AI8	8 MSB	R,W EEPROM		bit 0 – bit 3… channel 7 … bit 4 – bit 7… channel 8

input range for AI9, AI10	9 LSB	R,W EEPROM	**1 …Pt1000** (-50 to 150 °C) (-5000 to 15000), **divide by 100** to get the correct value **2 … voltage 0V … 10 V** (0 to 10000), **divide by 1000** to get the correct value **3 … resistance 0 … 1600 ohm** (0 to 16000), **divide by 10** to get the correct value **4 … current 0 … 20 mA** (0 to 20000), **divide by 1000** to get the correct value For 4…20 mA, jumper must be connected in parallel to the respective analogue input! **5 … resistance 0 – 5000 ohm** (0 to 50000), **divide by 10** to get the correct value.	bit 0 – bit 3… channel 9 … bit 4 – bit 7…channel 10
input range for AI11, AI12	9 MSB	R,W EEPROM		bit 0 – bit 3…channel 11 … bit 4 – bit 7…channel 12
input range for AI13, AI14	10 LSB	R,W EEPROM		bit 0 – bit 3…channel 13 … bit 4 – bit 7…channel 14
input range for AI15, AI16	10 MSB	R,W EEPROM		bit 0 – bit 3…channel 15 … bit 4 – bit 7…channel 16
latch state 1	11 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input 1 … bit 7 is input 8
latch state 2	11 MSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input 9 … bit 7 is input 16
latch state 3	12 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input 17 … bit 7 is input 24
latch state 4	12 MSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input 25 … bit 7 is input 32
relay com 1	13 LSB	R,W EEPROM	**0** – when no communication, relays stay in last state **1** – when no communication, relays are set to **relay state** values	bit 0 is relay 1 … bit 7 is relay 8

relay com 2	13 MSB	R,W EEPROM		bit 0 is relay 9 … bit 7 is relay 16

relay com 3	14 LSB	R,W EEPROM		bit 0 is relay 17 … bit 7 is relay 24
relay com 4	14 MSB	R,W EEPROM		bit 0 is relay 25 … bit 7 is relay 32
relay state 1	15 LSB	R,W EEPROM	relays go on or off (according to corresponding bits) if there was no communication with module for a given time and in **relay com** the corresponding relay bit is set to 1	bit 0 is relay 1 … bit 7 is relay 8
relay state 2	15 MSB	R,W EEPROM		bit 0 is relay 9 … bit 7 is relay 16
relay state 3	16 LSB	R,W EEPROM		bit 0 is relay 17 … bit 7 is relay 24
relay state 4	16 MSB	R,W EEPROM		bit 0 is relay 25 … bit 7 is relay 32
relay time 1	17 LSB	R,W EEPROM	time in [s] of no communication which is considered as communication failure	if set to 0 and no communication, the function is disabled
reserve 1	17 MSB	17 MSB	17 MSB	not used
relay start enable 1	18 LSB	R,W EEPROM	startup relay behaviour **0** – relays are not commanded **1** – the corresponding relay is set to its **relay start** value after module startup	bit 0 is relay 1 … bit 7 is relay 8
relay start enable 2	18 MSB	R,W EEPROM		bit 0 is relay 9 … bit 7 is relay 16
relay start enable 3	19 LSB	R,W EEPROM		bit 0 is relay 17 … bit 7 is relay 24
relay start enable 4	19 MSB	R,W EEPROM		bit 0 is relay 25 … bit 7 is relay 32
relay start 1	20 LSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 1 … bit 7 is relay 8

relay start 2	20 MSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 9 … bit 7 is relay 16
relay start 3	21 LSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 17 … bit 7 is relay 24

relay start 4	21 MSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is relay 25 … bit 7 is relay 32
latch enable 1	22 LSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after RESET the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits) inputs DI1-DI8
latch enable 2	22 MSB	R,W RAM		see register **latch enable 1** inputs DI9 – DI16
latch enable 3	23 LSB	R,W RAM		see register **latch enable 1** inputs DI17 – DI24
latch enable 4	23 MSB	R,W RAM		see register **latch enable 1** inputs DI25 – DI32
relay 1	24 LSB	R,W RAM	commands to control relay outputs **DO1-DO8**	bit 0 is relay 1 … bit 7 is relay 8
relay 2	24 MSB	R,W RAM	commands to control relay outputs **DO9-DO16**	bit 0 is relay 9 … bit 7 is relay 16
relay 3	25 LSB	R,W RAM	commands to control relay outputs **DO17-DO24**	bit 0 is relay 17 … bit 7 is relay 24
relay 4	25 MSB	R,W RAM	commands to control relay outputs **DO25-DO32**	bit 0 is relay 25 … bit 7 is relay 32
analogue outputs AO1	26 LSB 26 MSB	R,W RAM	the AO values are ranged 0000hex – 0FFFhex which is (0 dec – 4095dec) 0000hex is for 0V 0FFFhex is for 10V	analogue output channels
analogue outputs AO2	27 LSB 27 MSB	R,W RAM		
analogue outputs AO3	28 LSB 28 MSB	R,W RAM		

analogue outputs AO4	29 LSB 29 MSB	R,W RAM		
analogue outputs AO5	30 LSB 30 MSB	R,W RAM		
analogue outputs AO6	31 LSB 31 MSB	R,W RAM		
analogue outputs AO7	32 LSB 32 MSB	R,W RAM		
analogue outputs AO8	33 LSB 33 MSB	R,W RAM		

latched value 1	34 LSB	R	**catched values** **0 –** if since latch enable the latched state has not been detected at the input **1 -** if since latch enable the latched state has been detected at the input	reset of individual bits: disable and enable the corresponding bits – see register **latch enable** inputs **DI1-DI8**
latched value 2	34 MSB	R		reset of individual bits: disable and enable the corresponding bits – see register **latch enable** inputs **DI9-D**I16
latched value 3	35 LSB	R		reset of individual bits: disable and enable the corresponding bits – see register **latch enable** inputs **DI17-DI24**
latched value 4	35 MSB	R		reset of individual bits: disable and enable the corresponding bits – see register **latch enable** inputs **DI25-DI32**
inputs 1	36 LSB	R	readout of binary inputs **DI1-DI8**	bit 0 is input 1 … bit 7 is input 8
inputs 2	36 MSB	R	readout of binary inputs **DI9-DI16**	bit 0 is input 9 … bit 7 is input 16
inputs 3	37 LSB	R	readout of binary inputs **DI17-DI24**	bit 0 is input 17 … bit 7 is input 24
inputs 4	37 MSB	R	readout of binary inputs **DI24-DI32**	bit 0 is input 25 … bit 7 is input 32

channel value AI1	38 LSB 38 MSB	R	measured values at analogue inputs; scaling: see **input ranges** registers (regs. 7 to 10)	readouts of analogue inputs AI1..AI16
channel value AI2	39 LSB 39 MSB	R		
channel value AI3	40 LSB 40 MSB	R		
channel value AI4	41 LSB 41 MSB	R		
channel value AI5	42 LSB 42 MSB	R		
channel value AI6	43 LSB 43 MSB	R		
channel value AI7	44 LSB 44 MSB	R		
channel value AI8	45 LSB 45 MSB	R		
channel value AI9	46 LSB 46 MSB	R		
channel value AI10	47 LSB 47 MSB	R		
channel value AI11	48 LSB 48 MSB	R		
channel value AI12	49 LSB 49 MSB	R		

channel value AI13	50 LSB 50 MSB	R		
channel value AI14	51 LSB 51 MSB	R		
channel value AI15	52 LSB 52 MSB	R		
channel value AI16	53 LSB 53 MSB	R		
uptime	1000 LSB 1000MSB 1001 LSB 1001MSB	R	uptime [s]	