

### R320 – 16 OC transistor outputs

- **Bit address = 16 \* (word address - 1) + 1**
- **OC = open collector**
- **Supported Modbus functions: F01, F03, F15, F16**

Name	Address	Type (def)	Description	Note
module ID	1 LSB 1 MSB	R	module identification	Module ID: 8032hex
firmware	2 LSB 2 MSB	R	FW version	FW version (in dec) corresponds with version of this document; for example: FW 13h (19dec) = document V 01900 first three digits: FW version, remaining two digits: document revision
status LSB	3 LSB	R, W RAM	module status lower byte <b>bit 0</b> – EEPROM write enable <b>bit 1</b> – SW reset enable <b>bit 4</b> – EEPROM init <b>bit 5</b> – central write ban (all RW registers)	<b>EEPROM init</b> is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) <b>SW reset</b> Enables device restart (see register 1002)
status MSB	3 MSB	R	module status upper byte <b>bit 0</b> - 0 normal mode - 1 init mode <b>bit 1</b> - 1 at the next write attempt received data will be written to <b>EEPROM</b> - 0 at the next write attempt received data will be written to <b>RAM only</b> <b>bit 2</b> – 1 EEPROM initialised <b>bit 3</b> – central write disable indication <b>bit 4</b> – 0 <b>bit 5</b> – SW reset enable <b>bit 6</b> – 0 <b>bit 7</b> - 1	bit 3 ... central write ban indication – set by bit 5 in status LSB register

address	4 LSB	R, W EEPROM (1)	module address	!!! The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (comm speed)	4 MSB	R, W EEPROM (13)	10dec ... 1 200bps 11dec ... 2 400bps 12dec ... 4 800bps 13dec ... 9 600bps 14dec ... 19 200bps 15dec ... 38 400bps 16dec ... 57 600bps 17dec ... 115 200bps	!!! The changes will become active only after module restart (the register is written immediately, but the new baud rate is effective after restart only)
relay low	5 LSB	R, W RAM	OC outputs on / off	bit 0 is DO1 ... bit 7 is DO8
relay high	5 MSB	R, W RAM	OC outputs on / off	bit 0 is DO9 ... bit 7 is DO16
relay com low	6 LSB	R, W EEPROM (0)	<b>0</b> – when no communication, OCs stay in last state <b>1</b> – when no communication, OCs are set to <b>relay state</b> values	bit 0 is DO1 ... bit 7 is DO8
relay com high	6 MSB	R, W EEPROM (0)	<b>0</b> – when no communication, OCs stay in last state <b>1</b> – when no communication, OCs are set to <b>relay state</b> values	bit 0 is DO9 ... bit 7 is DO16
relay state	7 LSB	R, W EEPROM (0)	OCs go on or off (according to corresponding bits) if there was no communication with module for a given time and in <b>relay com</b> the corresponding relay bit is set to 1	bit 0 is DO1 ... bit 7 is DO8
relay state	7 MSB	R, W EEPROM (0)	OCs go on or off (according to corresponding bits) if there was no communication with module for a given time and in <b>relay com</b> the corresponding relay bit is set to 1	bit 0 is DO9 ... bit 7 is DO16

relay time	8 LSB	R, W EEPROM (30)	time in [s] of non-communication after which a OC is set in demanded state	if set to 0, the function is disabled
	8 MSB	R, RAM	reserved	
relay start enable low	9 LSB	R, W EEPROM (0)	startup OC behaviour <b>0</b> – relays are not commanded <b>1</b> – the corresponding relay is set to its <b>relay start</b> value after module startup	bit 0...is DO1 .. bit 7...is DO8
relay start enable high	9 MSB	R, W EEPROM (0)	startup OC behaviour <b>0</b> – relays are not commanded <b>1</b> – the corresponding relay is set to its <b>relay start</b> value after module startup	bit 0...is DO9 .. bit 7...is DO16
relay start low	10 LSB	R, W EEPROM (0)	OC state between power-up and first bus command	bit 0...is DO1 .. bit 7...is DO8
relay start high	10 MSB	R, W EEPROM (0)	OC state between power-up and first bus command	bit 0...is DO9 .. bit 7...is DO16
up time 1	11 LSB	R	time [in seconds] since module power-up or reset	LSB
up time 2	11 MSB	R		
up time 3	12 LSB	R		
up time 4	12 MSB	R		MSB
number EE values 1	13 LSB	R	number of EEPROM writing cycles (address, baud rate, range)	Counter 0 ... FFFh; no overflow, when FFFE is reached, the counter stops
number EE values 2	13 MSB	R		
uptime	1000 LSB 1000 MSB 1001 LSB 1001 MSB	R	uptime [s]	
SW reset	1002 LSB 1002 MSB	R, W RAM	writing of non-zero value executes module restart (function must be enabled in Status LSB bit 1).	
serial number	1003 LSB 1003 MSB 1004 LSB 1004 MSB	R, W EEPROM (0 – factory setting)	module serial number	
serial port settings	1005 LSB	R, W EEPROM (0)	serial port settings <b>bits 0,1</b> – parity 0 none 1 even 2 odd	<b>!!!</b> The changes will become active only after module restart



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# MODBUS

**R320**

16 × OC transistor outputs

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			<b>bit 2</b> - 0 one stopbit 1 two stopbits	
reserved	1005 MSB	R		
dip switch	1006 LSB	R	DIP switch actual value	
reserved	1006 MSB	R		

### Revision:

20. 09. 2017 ver. 100

14. 01. 2022 ver. 100 – stylistic adjustments, change logo