R420 – 16 × digital inputs

- **Bit address = 16 * (word address – 1) + 1**
- **Supported Modbus functions: F01, F03, F15, F16**

Name	Address	Type (def)	Description	Note
module ID	1 LSB 1 MSB	R	module identification	Module ID: 8042hex
firmware	2 LSB 2 MSB	R	FW version	FW version (in dec) corresponds with version of this document; for example: FW 13h (19dec) = document V 01900 first three digits: FW version, remaining two digits: document revision
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 1** – SW reset enable **bit 4** – EEPROM init **bit 5** – central write ban (all RW registers)	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **SW reset** Enables device restart (see register 1002)
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next write attempt received data will be written to **EEPROM** - 0 at the next write attempt received data will be written to **RAM only** **bit 2** – 1 EEPROM initialised **bit 3** – central write disable indication **bit 4** – 0 **bit 5** –SW reset enable **bit 6** – 0 **bit 7** - 1	bit 3 … central write ban indication – set by bit 5 in status LSB register

address	4 LSB	R,W EEPROM (1)	module address	**!!!** The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (comm speed)	4 MSB	R,W EEPROM (13)	10dec … 1 200bps 11dec … 2 400bps 12dec … 4 800bps 13dec … 9 600bps 14dec … 19 200bps 15dec … 38 400bps 16dec … 57 600bps 17dec … 115 200bps	**!!!** The changes will become active only after module restart (the register is written immediately, but the new baud rate is effective after restart)
inputs 1	5 LSB	R	readouts of the inputs	bit 0 is input DI1 … bit 7 is input DI8
inputs 2	5 MSB	R	readouts of the inputs	bit 0 is input DI9 … bit 7 is input DI16
latched value 1	6 LSB	R	catched values **0 –** if since latch enable the latched state **has not** been **detected** at the input **1 -** if since latch enable the latched state has been **detected** at the input	reset of individual bits: disable and enable the corresponding bits – see register **latch enable** bit 0 is input DI1 … bit 7 is input DI8
latched value 2	6 MSB	R	catched values **0 –** if since latch enable the latched state **has not** been **detected** at the input **1 -** if since latch enable the latched state has been **detected** at the input	reset of individual bits: disable and enable the corresponding bits – see register **latch enable** bit 0 is input DI9 … bit 7 is input DI16
latch state 1	7 LSB	R,W EEPROM (0)	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input DI1 … bit 7 is relay DI8
latch state 2	7 MSB	R,W EEPROM (0)	state to be catched **0** – log. 0 **1** - log. 1	bit 0 is input DI9 … bit 7 is relay DI16
latch enable 1	8 LSB	R,W RAM	latch function enable for each	reset the **latched value** register bits to

			input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after reset the register is set to 0	0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits) bit 0... input DI1 .. bit 7... input DI8
latch enable 2	8 MSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after reset the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits) bit 0... input DI9 .. bit 7... input DI16
up time 1	9 LSB	R	time [in seconds] since module power-up or reset	LSB
up time 2	9 MSB	R		
up time 3	10 LSB	R		
up time 4	10 MSB	R		MSB
number EE values 1	11 LSB	R	number of EEPROM writing cycles (address, baud rate, range)	counter 0 … FFFEh; no overflow, when FFFE is reached, the counter stops
number EE values 2	11 MSB	R		
uptime	1000 LSB 1000 MSB 1001 LSB 1001 MSB	R	uptime [s]	
SW reset	1002 LSB 1002 MSB	R, W RAM	writing of non-zero value executes module restart (function must be enabled in Status LSB bit 1).	
serial number	1003 LSB 1003 MSB 1004 LSB 1004 MSB	R, W EEPROM (0 – factory setting)	module serial number	
serial port settings	1005 LSB	R, W EEPROM (0)	serial port settings **bits 0,1** – parity 0 none 1 even 2 odd **bit 2** – 0 one stopbit 1 two stopbits	**!!!** The changes will become active only after module restart
reserved	1005 MSB	R		
dip switch	1006 LSB	R	DIP switch actual value	

reserved	1006 MSB	R		

Revision:

20. 09. 2017 ver. 100
14. 01. 2022 ver. 107 – stylistic adjustments, change logo