- **max 19 words may be read out as a whole (i.e. 38 bytes)**
- **the first 304 bits can be addressed bitwise (i.e. the whole map)**
- **supported modbus functions – F01, F03, F15, F16**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 8056hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware LSB	2 LSB	R	firmware version lower byte	FW version (in dec) corresponds with version of this document; for example: FW 13h (19 dec) = document V01900, first three digits: FW version, remaining two digits: document revision
firmware MSB	2 MSB	R	firmware version upper byte	
status LSB	3 LSB	R, W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 1** – enable SW reset **bit 2** – central write disable (all RW registers) **bit 4** – EEPROM init **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **SW reset** Enables device restart (see register 1002) **calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** change bit 7 from 1 to 0 and set bit 6 to 1
status MSB	3 MSB	R	module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be	

			written to RAM only **bit 2** EEPROM initialised **bit 3** calibration enabled **bit 4** – central write disable **bit 5** – SW reset enable **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	module address (0x01)	**!!!**The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
baud rate (comm speed)	4 MSB	R,W EEPROM	no parity 10_{dec} … 1200 bps 11_{dec} … 2400 bps 12_{dec} … 4800 bps 13_{dec} … 9600 bps 14_{dec} … 19200 bps 15_{dec} … 38400 bps 16_{dec} … 57600 bps 17_{dec} … 115200 bps	**!!!**The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
input range for inputs 1, 2	5 LSB	R,W EEPROM	**1 …Pt1000** (-50 to 150 °C) (-5000 to 15000), **divide by 100** to get the correct value **2 … voltage 0 V … 10 V** (0 to 10000), **divide by 1000** to get the correct value **3 … resistance 0 … 1600 Ohm** (0 to 16000), **divide by 10** to get the correct value **4 … current 0 … 20 mA** (0 to 20000), **divide by 1000** to get the correct value (AI 1-8: internal resistor 125 Ohm must be connected via DIP switch) **5 … resistance 0 – 5000 Ohm** (0 to 50000), **divide by 10** to get the correct value.	bit 0 to bit 3: input 1 bit 4 to bit 7: input 2
input range for inputs 3, 4	5 MSB	R,W EEPROM		bit 0 to bit 3: input 3 bit 4 to bit 7: input 4
input range for inputs 5, 6	6 LSB	R,W EEPROM		bit 0 to bit 3: input 5 bit 4 to bit 7: input 6
input range for inputs 7, 8	6 MSB	R,W EEPROM		bit 0 to bit 3: input 7 bit 4 to bit 7: input 8
input 1 value	7 LSB, 7 MSB	R	0 to maximum range, see above ($0 … 65535_{dec}$; 0000 – $FFFF_{hex}$)	Measured values on input channels
input 2 value	8 LSB, 8 MSB	R		
input 3 value	9 LSB, 9 MSB	R		

input 4 value	10 LSB, 10 MSB	R		
input 5 value	11 LSB, 11 MSB	R		
input 6 value	12 LSB, 12 MSB	R		
input 7 value	13 LSB, 13 MSB	R		
input 8 value	14 LSB, 14 MSB	R		
channels	15 LSB	R	Measured channels **log. 0** on bit means that the respective channel **will not** be sampled **log. 1 ...** means that the respective channel **will be** sampled **bit 0** input channel 1 (AI1) **bit 1** input channel 2 (AI2) **...** **bit 7 ...** input channel 8 (AI8)	Not implemented yet
reserved	15 MSB			
uptime 1	16 LSB	R	time in seconds since module power-up or reset	LSB
uptime 2	16 MSB	R		
uptime 3	17 LSB	R		
uptime 4	17 MSB	R		MSB
number of EE write cycles - values 1	18 LSB	R	number of EEPROM writing cycles (address, baud rate, range...), just for information	counter 0...FFFE; no overflow. When FFFE is reached, the counter stops.
number of EE write cycles - values 2	18 MSB	R		
number of EE write cycles - calibration 1	19 LSB	R	number of EEPROM writing cycles - calibration	counter 0...FFFE; no overflow. When FFFE is reached, the counter stops.
number of EE write cycles – calibration 2	19 MSB	R		
uptime	1000 LSB 1000 MSB 1001 LSB 1001 MSB	R	Uptime [s]	
SW reset	1002 LSB 1002 MSB	R, W RAM	Writing of a non-zero value executes SW reset (function must be enabled in Status LSB bit 1).	
serial number	1003 LSB 1003 MSB 1004 LSB 1004 MSB	R	Module serial number	

serial port settings	1005 LSB	R, W EEPROM	Settings of serial port **bits 0,1** – parity 0 – none 1 – even 2 – odd **Bit 2** – 0 – one stopbit 1 – two stopbits	**!!!**The changes will become active only after module restart (the register is written immediately, but the new address is effective after restart)
reserved	1005 MSB	R		
DIP switch	1006 LSB	R	Actual value of the addressing DIP switch – for diagnostics only	
reserved	1006 MSB	R		