

## RXIO Modbus – 16 × AI (voltage, current, resistance), 8 × AO, 32 × DI, 32 × relay outputs

- max 53 words may be read out as a whole (i.e. 106 bytes)
- first 848 bits can be addressed bitwise (i.e. 1LSB – 53MSB)
- Supported Modbus functions: F01, F03, F15, F16

| Name             | Address | Type     | Description   | Note   |
|------------------|---------|----------|---|--|
| module ID<br>LSB | 1 LSB   | R        | module identification lower byte  | module ID is 8103hex   |
| module ID<br>MSB | 1 MSB   | R        | module identification upper byte  |  |
| firmware<br>LSB  | 2 LSB   | R        | lower byte FW version   | 8hex   |
| firmware<br>MSB  | 2 MSB   | R        | upper byte FW version   |  |
| status LSB       | 3 LSB   | R, W RAM | module status lower byte<br><b>bit 0</b> – EEPROM write enable<br><b>bit 4</b> – EEPROM init  | <b>EEPROM init</b><br>is enabled when the<br>INIT switch was ON at<br>power-up, and switched<br>OFF before bit 4 was<br>set to 1 (indicated by<br>bit 2 in status MSB) |
| status MSB       | 3 MSB   | R        | module status upper byte<br><b>bit 0</b> - 0 normal mode<br>- 1 init mode<br><b>bit 1</b> - 1 at the next EEPROM<br>write attempt all data will be<br>saved to EEPROM<br>- 0 at the next write<br>attempt received data will be<br>written to RAM only<br><b>bit 2</b> – 1 – EPROM initialised<br><b>bit 4</b> – 0 –correct on-board<br>I2C communication between<br>processor and peripherals<br>- 1 –incorrect on-board<br>I2C communication between<br>processor and peripherals<br><b>bit 5</b> - 1<br><b>bit 6</b> - 0<br><b>bit 7</b> - 1 |  |

|         |       |                       |                       |   |
|---------|-------|-----------------------|-----------------------|---|
| address | 4 LSB | R, W<br>EEPROM<br>(1) | Modbus module address | <b>!!!</b> the change will be effective after restart only (however the register will be set immediately) |
|---------|-------|-----------------------|-----------------------|---|

|                          |       |   |   |  |
|--------------------------|-------|---|---|--|
| baud rate                | 4 MSB | R, W<br>EEPROM<br>(13dec)                             | no parity communication<br>10dec ... 1200bps<br>11dec ... 2400bps<br>12dec ... 4800bps<br>13dec ... 9600bps<br>14dec ... 19200bps   | <b>!!!</b> the change will be effective after restart only (however the register will be set immediately)  |
| calibration 1            | 5 LSB | R, W RAM  | register to calibrate analogue inputs 1-8<br><b>bit 5</b> – calibration offset<br><b>bit 6</b> – calibration span<br><b>bit 7</b> – calibration enable  | <b>calibration</b> is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB)<br><b>calibration offset</b><br>change bit 7 from 1 to 0 and set bit 5 to 1<br><b>calibration span</b><br>change bit 7 from 1 to 0 and set bit 6 to 1 |
| calibration 1            | 5 MSB | R, W RAM  | <b>bit 3</b> – 1 - calibration enable   | indicates enabled calibration of analogue inputs 1-8   |
| calibration 2            | 6 LSB | R, W RAM  | register to calibrate analogue inputs 9-16<br><b>bit 5</b> – calibration offset<br><b>bit 6</b> – calibration span<br><b>bit 7</b> – calibration enable   | function is same as calibration 1 LSB  |
| calibration 2            | 6 MSB | R, W RAM  | bit 3 – 1 - calibration enable  | indicates enabled calibration of analogue inputs 9-16  |
| input range for AI1, AI2 | 7 LSB | R, W<br>EEPROM<br>(0x33, inputs set for 0...1600 ohm) | <b>1 ...Pt1000</b> (-50 to 150 °C) (-5000 to 15000), <b>divide by 100</b> to get the correct value<br><b>3 ... resistance 0 ... 1600 ohm</b> (0 to 16000), <b>divide by 10</b> to get the correct value<br><b>5 ... resistance 0 – 5000 ohm</b> (0 to 50000), <b>divide by 10</b> to get the correct value. | bit 0 – bit 3...channel 1<br>...<br>bit 4 – bit 7... channel 2   |
| input range for AI3, AI4 | 7 MSB | R, W<br>EEPROM<br>(0x33, inputs set for               |   | bit 0 – bit 3... channel 3<br>...<br>bit 4 – bit 7... channel 4  |



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## RXIO – Compact I/O module

16 × AI, 8 × AO, 32 × relay outputs,  
32 × DI

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|                            |        |   |  |   |
|----------------------------|--------|---|--|---|
|                            |        | 0...1600 ohm)                                   |  |   |
| input range for AI5, AI6   | 8 LSB  | R, W EEPROM (0x33, inputs set for 0...1600 ohm) |  | bit 0 – bit 3... channel 5<br>...<br>bit 4 – bit 7... channel 6 |
| input range for AI7, AI8   | 8 MSB  | R, W EEPROM (0x33, inputs set for 0...1600 ohm) |  | bit 0 – bit 3... channel 7<br>...<br>bit 4 – bit 7... channel 8 |
| input range for AI9, AI10  | 9 LSB  | R, W EEPROM (0x22, inputs set for 0...10V)      | <p><b>1 ...Pt1000</b> (-50 to 150 °C) (-5000 to 15000), <b>divide by 100</b> to get the correct value</p> <p><b>2 ... voltage 0V ... 10 V</b> (0 to 10000), <b>divide by 1000</b> to get the correct value</p> <p><b>3 ... resistance 0 ... 1600 ohm</b> (0 to 16000), <b>divide by 10</b> to get the correct value</p> <p><b>4 ... current 0 ... 20 mA</b> (0 to 20000), <b>divide by 1000</b> to get the correct value<br/>For 4...20 mA, jumper must be connected in parallel to the respective analogue input!</p> <p><b>5 ... resistance 0 – 5000 ohm</b> (0 to 50000), <b>divide by 10</b> to get the correct value.</p> | bit 0 – bit 3... channel 9<br>...<br>bit 4 – bit 7...channel 10 |
| input range for AI11, AI12 | 9 MSB  | R, W EEPROM (0x22, inputs set for 0...10V)      |  | bit 0 – bit 3...channel 11<br>...<br>bit 4 – bit 7...channel 12 |
| input range for AI13, AI14 | 10 LSB | R, W EEPROM (0x22, inputs set for 0...10V)      |  | bit 0 – bit 3...channel 13<br>...<br>bit 4 – bit 7...channel 14 |
| input range for AI15, AI16 | 10 MSB | R, W EEPROM (0x22, inputs set for 0...10V)      |  | bit 0 – bit 3...channel 15<br>...<br>bit 4 – bit 7...channel 16 |

|               |        |                          |  |  |
|---------------|--------|--------------------------|--|--|
| latch state 1 | 11 LSB | R, W<br>EEPROM<br>(0x00) | state to be caught<br><b>0</b> – log. 0<br><b>1</b> – log. 1   | bit 0 is input 1<br>...<br>bit 7 is input 8                      |
| latch state 2 | 11 MSB | R, W<br>EEPROM<br>(0x00) | state to be caught<br><b>0</b> – log. 0<br><b>1</b> – log. 1   | bit 0 is input 9<br>...<br>bit 7 is input 16                     |
| latch state 3 | 12 LSB | R, W<br>EEPROM<br>(0x00) | state to be caught<br><b>0</b> – log. 0<br><b>1</b> – log. 1   | bit 0 is input 17<br>...<br>bit 7 is input 24                    |
| latch state 4 | 12 MSB | R, W<br>EEPROM<br>(0x00) | state to be caught<br><b>0</b> – log. 0<br><b>1</b> – log. 1   | bit 0 is input 25<br>...<br>bit 7 is input 32                    |
| relay com 1   | 13 LSB | R, W<br>EEPROM<br>(0x00) | <b>0</b> – when no communication,<br>relays stay in last state<br><b>1</b> – when no communication,<br>relays are set to <b>relay state</b><br>values  | bit 0 is relay 1<br>...<br>bit 7 is relay 8                      |
| relay com 2   | 13 MSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 9<br>...<br>bit 7 is relay 16                     |
| relay com 3   | 14 LSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 17<br>...<br>bit 7 is relay 24                    |
| relay com 4   | 14 MSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 25<br>...<br>bit 7 is relay 32                    |
| relay state 1 | 15 LSB | R, W<br>EEPROM<br>(0x00) | relays go on or off (according to<br>corresponding bits) if there was<br>no communication with module<br>for a given time and in <b>relay</b><br><b>com</b> the corresponding relay bit<br>is set to 1 | bit 0 is relay 1<br>...<br>bit 7 is relay 8                      |
| relay state 2 | 15 MSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 9<br>...<br>bit 7 is relay 16                     |
| relay state 3 | 16 LSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 17<br>...<br>bit 7 is relay 24                    |
| relay state 4 | 16 MSB | R, W<br>EEPROM<br>(0x00) |  | bit 0 is relay 25<br>...<br>bit 7 is relay 32                    |
| relay time 1  | 17 LSB | R, W<br>EEPROM           | time in [s] of no<br>communication which is<br>considered as<br>communication failure  | if set to 0 and no<br>communication, the<br>function is disabled |
| reserved      | 17 MSB |                          |  | not used   |

|                      |        |                    |  |  |
|----------------------|--------|--------------------|--|--|
| relay start enable 1 | 18 LSB | R, W EEPROM (0x00) | startup relay behaviour<br><b>0</b> – relays are not commanded<br><b>1</b> – the corresponding relay is set to its <b>relay start</b> value after module startup                           | bit 0 is relay 1<br>...<br>bit 7 is relay 8  |
| relay start enable 2 | 18 MSB | R, W EEPROM (0x00) |  | bit 0 is relay 9<br>...<br>bit 7 is relay 16   |
| relay start enable 3 | 19 LSB | R, W EEPROM (0x00) |  | bit 0 is relay 17<br>...<br>bit 7 is relay 24  |
| relay start enable 4 | 19 MSB | R, W EEPROM (0x00) |  | bit 0 is relay 25<br>...<br>bit 7 is relay 32  |
| relay start 1        | 20 LSB | R, W EEPROM (0x00) | relay status between power-up and first bus command  | bit 0 is relay 1<br>...<br>bit 7 is relay 8  |
| relay start 2        | 20 MSB | R, W EEPROM (0x00) | relay status between power-up and first bus command  | bit 0 is relay 9<br>...<br>bit 7 is relay 16   |
| relay start 3        | 21 LSB | R, W EEPROM (0x00) | relay status between power-up and first bus command  | bit 0 is relay 17<br>...<br>bit 7 is relay 24  |
| relay start 4        | 21 MSB | R, W EEPROM (0x00) | relay status between power-up and first bus command  | bit 0 is relay 25<br>...<br>bit 7 is relay 32  |
| latch enable 1       | 22 LSB | R, W RAM           | latch function enable for each input – if set to <b>1</b> the <b>latched value</b> bit goes to 0 and stays so until the latched value is detected;<br>after RESET the register is set to 0 | reset the <b>latched value</b> register bits to 0 by changing the value of <b>latch enable</b> bits from 0 to 1 (= disable and enable latching for individual bits) inputs DI1-DI8 |
| latch enable 2       | 22 MSB | R, W RAM           |  | see register <b>latch enable 1</b> inputs DI9 – DI16   |
| latch enable 3       | 23 LSB | R, W RAM           |  | see register <b>latch enable 1</b> inputs DI17 – DI24  |
| latch enable 4       | 23 MSB | R, W RAM           |  | see register <b>latch enable 1</b> inputs DI25 – DI32  |
| relay 1              | 24 LSB | R, W RAM           | commands to control relay outputs <b>DO1-DO8</b>   | bit 0 is relay 1<br>...<br>bit 7 is relay 8  |



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16 × AI, 8 × AO, 32 × relay outputs,  
32 × DI

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|                      |                  |          |  |  |
|----------------------|------------------|----------|--|--|
| relay 2              | 24 MSB           | R, W RAM | commands to control relay outputs <b>D09-D016</b>  | bit 0 is relay 9<br>...<br>bit 7 is relay 16   |
| relay 3              | 25 LSB           | R, W RAM | commands to control relay outputs <b>D017-D024</b>   | bit 0 is relay 17<br>...<br>bit 7 is relay 24  |
| relay 4              | 25 MSB           | R, W RAM | commands to control relay outputs <b>D025-D032</b>   | bit 0 is relay 25<br>...<br>bit 7 is relay 32  |
| analogue outputs AO1 | 26 LSB<br>26 MSB | R, W RAM | the AO values are ranged 0000hex – 0FFFhex which is (0 dec – 4095dec)<br><br>0000hex is for 0V<br>0FFFhex is for 10V   | analogue output channels   |
| analogue outputs AO2 | 27 LSB<br>27 MSB | R, W RAM |  |  |
| analogue outputs AO3 | 28 LSB<br>28 MSB | R, W RAM |  |  |
| analogue outputs AO4 | 29 LSB<br>29 MSB | R, W RAM |  |  |
| analogue outputs AO5 | 30 LSB<br>30 MSB | R, W RAM |  |  |
| analogue outputs AO6 | 31 LSB<br>31 MSB | R, W RAM |  |  |
| analogue outputs AO7 | 32 LSB<br>32 MSB | R, W RAM |  |  |
| analogue outputs AO8 | 33 LSB<br>33 MSB | R, W RAM |  |  |
| latched value 1      | 34 LSB           | R        | <b>atched values</b><br><b>0</b> – if since latch enable the latched state has not been detected at the input<br><b>1</b> - if since latch enable the latched state has been detected at the input | reset of individual bits: disable and enable the corresponding bits – see register <b>latch enable</b> inputs <b>DI1-DI8</b>   |
| latched value 2      | 34 MSB           | R        |  | reset of individual bits: disable and enable the corresponding bits – see register <b>latch enable</b> inputs <b>DI9-DI16</b>  |
| latched value 3      | 35 LSB           | R        |  | reset of individual bits: disable and enable the corresponding bits – see register <b>latch enable</b> inputs <b>DI17-DI24</b> |
| latched value 4      | 35 MSB           | R        |  | reset of individual bits: disable and enable the corresponding bits – see register <b>latch enable</b>                         |

|                    |                  |   |  |   |
|--------------------|------------------|---|--|---|
|                    |                  |   |  | inputs <b>DI25-DI32</b>                       |
| inputs 1           | 36 LSB           | R | readout of binary inputs<br><b>DI1-DI8</b>   | bit 0 is input 1<br>...<br>bit 7 is input 8   |
| inputs 2           | 36 MSB           | R | readout of binary inputs<br><b>DI9-DI16</b>  | bit 0 is input 9<br>...<br>bit 7 is input 16  |
| inputs 3           | 37 LSB           | R | readout of binary inputs<br><b>DI17-DI24</b>   | bit 0 is input 17<br>...<br>bit 7 is input 24 |
| inputs 4           | 37 MSB           | R | readout of binary inputs<br><b>DI24-DI32</b>   | bit 0 is input 25<br>...<br>bit 7 is input 32 |
| channel value AI1  | 38 LSB<br>38 MSB | R | measured values at analogue inputs; scaling: see <b>input ranges</b> registers (regs. 7 to 10) | readouts of analogue inputs AI1..AI16         |
| channel value AI2  | 39 LSB<br>39 MSB | R |  |   |
| channel value AI3  | 40 LSB<br>40 MSB | R |  |   |
| channel value AI4  | 41 LSB<br>41 MSB | R |  |   |
| channel value AI5  | 42 LSB<br>42 MSB | R |  |   |
| channel value AI6  | 43 LSB<br>43 MSB | R |  |   |
| channel value AI7  | 44 LSB<br>44 MSB | R |  |   |
| channel value AI8  | 45 LSB<br>45 MSB | R |  |   |
| channel value AI9  | 46 LSB<br>46 MSB | R |  |   |
| channel value AI10 | 47 LSB<br>47 MSB | R |  |   |
| channel value AI11 | 48 LSB<br>48 MSB | R |  |   |
| channel value AI12 | 49 LSB<br>49 MSB | R |  |   |
| channel value AI13 | 50 LSB<br>50 MSB | R |  |   |
| channel value AI14 | 51 LSB<br>51 MSB | R |  |   |
| channel value AI15 | 52 LSB<br>52 MSB | R |  |   |
| channel value AI16 | 53 LSB<br>53 MSB | R |  |   |



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|        |  |   |            |  |
|--------|--|---|------------|--|
| uptime | 1000 LSB<br>1000MSB<br>1001 LSB<br>1001MSB | R | uptime [s] |  |
|--------|--|---|------------|--|





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## Revision:

14. 12. 2017 ver. 100

14. 01. 2022 ver. 102 – stylistic adjustments, change logo