UI410 Modbus table
signalling I/O module

Release 21.9.2011 ver. 00300

domat control system

- **max 13 words may be read out as a whole (i.e. 26 bytes)**
- **first 256 bits can be addressed bitwise (i.e. 1 LSB – 16 MSB)**

Name	Address	Type	Description	Note
module ID LSB	1 LSB	R	module identification lower byte	module ID is 0410hex
module ID MSB	1 MSB	R	module identification upper byte	
firmware	2 LSB 2 MSB	R	FW version	3hex
status LSB	3 LSB	R,W RAM	module status lower byte **bit 0** – EEPROM write enable **bit 4** – EEPROM init **bit 5** – calibration offset **bit 6** – calibration span **bit 7** – calibration enable	**EEPROM init** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 4 was set to 1 (indicated by bit 2 in status MSB) **calibration** is enabled when the INIT switch was ON at power-up, and switched OFF before bit 7 was set to 1 (indicated by bit 3 in status MSB) **calibration offset** change bit 7 from 1 to 0 and set bit 5 to 1 **calibration span** change bit 7 from 1 to 0 and set bit 6 to 1
status MSB	3 MSB		module status upper byte **bit 0** - 0 normal mode - 1 init mode **bit 1** - 1 at the next EEPROM write attempt all data will be saved to EEPROM - 0 at the next write attempt received data will be written to RAM only **bit 2** – 1 – EPROM initialised **bit 3** – 1 – calibration enabled **bit 4** - 0 **bit 5** - 1 **bit 6** - 0 **bit 7** - 1	
address	4 LSB	R,W EEPROM	module Modbus RTU address	**!!!**The changes will become active only after

				module restart (the register is written immediately, but the new address is effective after restart)

baud rate (comm speed)	4 MSB	R,W EEPROM	no parity 10_{dec} … 1200 bps 11_{dec} … 2400 bps 12_{dec} … 4800 bps 13_{dec} … 9600 bps 14_{dec} … 19200 bps 15_{dec} … 38400 bps 16_{dec} … 57600 bps 17_{dec} … 115200 bps	**!!!**The changes will become active only after module restart (the register is written immediately, the new baud rate is effective after restart)
latch state	5 LSB	R,W EEPROM	state to be catched **0** – log. 0 **1** - log. 1	
relay com	5 MSB	R,W EEPROM	**0** – when no communication, relays stay in last state **1** – when no communication, relays are set to **relay state** values	bit 0 is SSR bit 1 is LED bit 2 is beeper
relay state	6 LSB	R,W EEPROM	relays go on or off (according to corresponding bits) if there was no communication with module for a given time and in **relay com** the corresponding relay bit is set to 1	bit 0 is SSR bit 1 is LED bit 2 is beeper
relay time	6 MSB	R,W EEPROM	time in [s] of no communication which is considered as communication failure	if set to 0, the function is disabled
relay start enable	7 LSB	R,W EEPROM	startup relay behaviour **0** – relays are not commanded **1** – the corresponding relay is set to its **relay start** value after module startup	bit 0 is SSR bit 1 is LED bit 2 is beeper
relay start	7 MSB	R,W EEPROM	relay status between power-up and first bus command	bit 0 is SSR bit 1 is LED bit 2 is beeper
time LED 0	8 LSB	R,W EEPROM	LED flashing period (off)	in ms*10 range: 10 ms.... 10s
time LED 1	8 LSB	R,W EEPROM	LED flashing period (on)	in ms*10 range: 10 ms.... 10s
time BEEP 0	9 LSB	R,W EEPROM	beeper silence period (off)	in ms*10 range: 10 ms.... 10s
time BEEP 1	9 MSB	R,W EEPROM	beeper sound period (on)	in ms*10 range: 10 ms.... 10s

relay	10 LSB	R,W RAM	outputs on/off	bit 0 is SSR bit 1 is LED bit 2 is beeper
latch enable	10 MSB	R,W RAM	latch function enable for each input – if set to **1** the **latched value** bit goes to 0 and stays so until the latched value is detected; after RESET the register is set to 0	reset the **latched value** register bits to 0 by changing the value of **latch enable** bits from 0 to 1 (= disable and enable latching for individual bits)
inputs	11 LSB	R	binary input readout	bit 0 is DI 1
latched values	11 MSB	R	catched values **0 –** if since latch enable the latched state has not been detected at the input **1 -** if since latch enable the latched state has been detected at the input	bit 0 is DI 1 reset of individual bits: disable and enable the corresponding bits – see register **latch enable**
Pt1000 temp	12 LSB 12 MSB	R	actual external temperature measured by the Pt1000 sensor (*100, with offset 50 °C. Min value 0 ... –50 °C, max. value 15000 ... 100 °C	unsigned register, recalculation: temperature = (read value / 100) – 50 -50.00 °C ... 0 20.00 °C ... 7000
internal temp	13 MSB 13 LSB	R	actual internal temperature (*10)	recalculate: set temperature = read value / 10 0 … 0 199.9 … 1999 -0.1 … 0FFFFhex -199.9 … 0F831hex